Symmetricom

bc635VME/bc350VXI Time and Frequency Processor

Revision E

User's Guide

8500-0019

January, 2004

bc635VME/bc350VXI
TIME AND FREQUENCY PROCESSOR

TABLE OF CONTENTS

SECTION	PAGE

CHAPTER ONE
INTRODUCTION

CHAPTER TWO
INSTALLATION AND SETUP

CHAPTER THREE
INTERFACES

CHAPTER FOUR
FIFO DATA PACKETS

CHAPTER FIVE
PROGRAMMING EXAMPLES

CHAPTER SIX
INPUTS AND OUTPUTS

CHAPTER SEVEN
ADJUSTMENTS

This Page Intentionally Left Blank.

CHAPTER ONE

INTRODUCTION

1.0 GENERAL

The bc635VME/bc350VXI Time and Frequency Processor User's Guide provides the following information:

- Introduction and key feature description.
- Installation and setup.
- Detailed operation and programming interfaces.
- Input and output signals.
- Programming examples.

1.1 KEY FEATURES

The Time and Frequency Processor (TFP) has been designed with the following key features:

- Time on demand (days through 0.1 microseconds) with zero latency. This feature is implemented with hardware registers which latch the current time upon host request.
- Event logging (days through 0.1 microseconds). This feature is implemented with a second set of hardware registers. Time is captured on a positive or negative input edge.
- Six operational modes are supported. Modes are distinguished by the reference source.

Mode	Source Of Synchronization
0	Timecode – IRIG-A IRIG-B XR3 2137 NASA 36
1	Free running - on board VCXO used as reference.
2	1 PPS - accepts input one pulse per second.
3	RTC - uses battery backed on board real time clock IC.
5	GPS (optional) - double wide configuration including GPS receiver. (obsolete)
6	GPS (optional) - uses GPS receiver/antenna (receiver in antenna).

- Provides an output clock synchronized to the selected reference; programmable 1, 5, or 10MHz TTL.

- All modes of operation are supplemented by flywheel operation. For example, if synchronization source is lost, the TFP will continue to function at the last known reference rate.

- Generates synchronized IRIG B timecode. Modulated and DC level shift formats are produced simultaneously. Also generates IRIG H DC level shift.

- Programmable frequency output (periodics) is provided. The output frequency is 10,000,000 / (n1 * n2). 1<n1<65536 & 1<n2<65536.

- A time coincidence strobe output is provided. Programmable from hours through milliseconds. This strobe also has an each second mode programmable to milliseconds.

- Five maskable interrupt sources are supported. IRQ levels one through seven are programmable.

Int. #	Source Of Interrupt
0	External event input has occurred.
1	Periodic output has occurred.
2	Time coincidence strobe has occurred.
3	One second epoch (1PPS output) has occurred.
4	Output data packet is available.

- Time-of-day, hours, minutes, and seconds are displayed on front panel LED's.

- Most inputs and outputs are accessible via the P2 connector.

1.2 PHYSICAL OVERVIEW

The TFP is a B size module (6U X 160 mm). Operation is controlled by a block of thirty-two D16 registers written and read by the host via the VMEbus (A16 : D16). The TFP is available in two versions. The bc635VME is intended for use in a VMEbus system with most I/O signals available on rows A and C of the P2 connector. The bc350VXI is intended for use in a VXIbus system, and is shipped without a P2 connector. A dip switch is used to select VME or VXI compatibility. In VMEbus systems the register block can be located on any 64 byte boundary. In VXIbus systems the register block can be located at any of the 256 logical addresses (A15 and A14 must be high). The logical address is returned during an interrupt acknowledge cycle.

1.3 SPECIFICATIONS

1.3.1 TIMECODE READER

Format – AM	IRIG B XR3 2137 NASA 36.
Carrier Range	+/- 50ppm.
Modulation Ratio	3:1 to 6:1.
Input Amplitude	0.5 to 5 volts peak to peak.
Input Impedance	10KΩ AC coupled.

Format - DCLS	IRIG A IRIG B NASA 36.
Carrier Range	+/- 50ppm.
Input Amplitude	TTL/CMOS Compatible
Input Impedance	10KΩ DC coupled.

1.3.2 TIMECODE GENERATOR

Format - AM	IRIG B.
Modulation Ratio	3:1.
Output Amplitude	0 to 10 volts peak to peak, adjusted by VR1, into 50Ω.

Format - DCLS	IRIG B IRIG H
DC Level Shift	TTL/CMOS compatible, into 50Ω.

1.3.3 BUS CHARACTERISTICS

Address Space	A16, AM codes $29 and $2D, 64 bytes.
Data Transfer	D16.
Interrupter	D08(0), I(1-7), ROAK.
Power	+5 @ 1.5amps +12 @ 50 milliamp -12 @ 30 milliamp

1.3.4 DIGITAL INPUTS

Event Capture	TTL/CMOS positive or negative edge triggered.
	20 nanoseconds minimum width 250 nanoseconds minimum period.
	Input impedance 10KΩ

External 1PPS	TTL/CMOS positive edge on time.
	Twenty nanoseconds minimum width.
	Input impedance 10KΩ

1.3.5 EXTERNAL 10MHz INPUT/OUTPUT

10MHz Input	TTL/CMOS 45% To 55% Duty Cycle.
	1.5 To 4 Volts Peak-To-Peak, AC coupled 2.5KHz impedance.

Note: When an ovenized onboard oscillator is used, the external 10MHz input feature is disabled. Instead the output of the ovenized oscillator appears on this pin. It can only drive a single high impedance load.

1.3.6 DIGITAL OUTPUTS

1PPS	TTL/CMOS positive edge on time, 200mS positive pulse, into 50Ω.
Periodics	TTL/CMOS positive edge on time, into 50Ω. (See section 4.1.5)
Strobe	TTL/CMOS positive edge on time, 1mS positive pulse, into 50Ω.
1, 5, 10MHz Clock	TTL/CMOS positive edge on time, 5 & 10MHz square wave, 1MHz 80/20 duty cycle, into 50Ω.

1.3.7 OSCILLATOR CONTROL OUTPUT

Control Range	0 – 5V
Transfer Coefficient	Positive

1.4 ENVIRONMENTAL SPECIFICATIONS

Temperature	Operating	0 to 70^{o} centigrade.
	Non-Operating	-30 to +85^{o} centigrade.
Relative Humidity	Operating	85% @ +85 ^{o} C, 1000 hours.
Altitude	Operating	-400 to 18,000 meters MSL.

1.5 FUNCTIONAL OVERVIEW

This section describes the functions provided by the bc635VME/bc350VXI Time and Frequency Processor (TFP).

1.5.1 TIME

This function controls how the TFP card acquires and maintains time data. These functions allow the user to select where to obtain time data, whether or not to manipulate the time data and how to present the time data to the user system.

1.5.1.1 TIME SYNC MODE

This allows the user to select the operating mode (time source) of the TFP device. Available modes are Time Code Decoding, Freerunning, External 1PPS, RTC & GPS (Optional).

1.5.1.2 TIME FORMAT

The event time capture and time registers of the TFP default to the decimal time format. The major time registers are divided into 4 bit fields for each decimal digit of days, hours minutes and seconds. For the GPS mode only, the time registers can operate in the binary format where major time is represented as seconds since the GPS epoch.

1.5.1.3 SET TIME

This function allows the user to set the time on the TFP device. Decimal time values can be entered into the time registers. This function is typically used when operating in either the Freerunning or External 1PPS modes. While the function may be used when operating in Time code or GPS modes, subsequent time data received from the selected reference source will overwrite the loaded time.

1.5.1.4 SET YEAR

This function allows the user to set the year data. Typically, this function is used when the board is operating in time code decoding mode. Many time code formats (including standard IRIG B) do not include year information in the data. Using this function will allow the TFP device to extract the time of year data from the time code source while using year information provided by the user. The board will decode the year and roll over the days for a leap year (365-366-001) or a non-leap year (365-001). The supported range is 1990 – 2037. The board will follow the input time source if the input rollover day sequence does not match the board rollover day sequence as defined by the programmed year.

1.5.1.5 SET LOCAL OFFSET

This function allows the user to program a local offset of 1-hour increments into the TFP device. If the local offset value is nonzero, the device will adjust any reference timing information in order to maintain a local time in TFP clock. Use of this function only affects the time data in the TIME registers described in paragraph 3.1.

1.5.1.6 SET PROPAGATION DELAY

This function allows the user to command the TFP device to compensate for propagation delays introduced by the currently selected reference source. For example, when the unit is operating in Time code decoding mode, a long cable run could result in the input time code having a propagation delay. The delay value is programmable in units of 100ns and has an allowed range from –9999999 through +9999999.

1.5.1.7 DAYS

When a time source signal is not present at board power up, the board will begin counting at day 000. The TFP can be operated to count days in two modes. For the default Day 000 Invalid Mode, the TFP will not accept an input day of 000. Table 1 shows the possible combinations of input source data and current board state on the left side, and the result of the day rollover on the right side. Note that the table includes such combinations as where the board is set to a non-leap year, but the source is in a leap year.

Table 1 Day 000 Invalid Mode

Combination number	Board year	Input mode	Source Year	Source day	Board year	Board day	Notes
1.1.1	99	Timecode	N/A	000	99	Freerun	lost track
1.1.2	99	Timecode	99	365 – 001	99 - 00	365 – 001	
1.1.3	99	Timecode	00	366 – 001	99 - 00	366 – 001	
1.2.1	99	Freerun	N/A	365	99 - 00	365 – 001	
1.2.2	99	Freerun	N/A	366	99 - 00	366 – 001	
2.1.1	00	Timecode	00	365 – 366	00	365 – 366	
2.1.2	00	Timecode	99	365 – 001	00	365 – 001	1
2.1.3	00	Timecode	00	366 – 001	00 - 01	366 – 001	
2.2.1	00	Freerun	N/A	365	00	365 – 366	
2.2.2	00	Freerun	N/A	366	01	366 – 001	

Note 1: Day went to 366 for about one second, then went to day 001

For the optional Accept Day 000 Mode, the TFP will accept an input source with an input day of 000. Table 2 shows the possible combinations for this mode.

Table 2 Accept Day 000 Mode

Combination number	Board year	Input mode	Input Year	Input day	Board year	Board day	Notes
3.1.1	99	Timecode	N/A	000	99	000 – 001	
3.1.2	99	Timecode	99	364 – 365	99	364 – 365	
3.1.3	99	Timecode	99	365 – 001	99 – 00	365 – 001	***2***
3.1.4	99	Timecode	00	365 – 366	99 – 00	365 – 366	***2***
3.1.5	99	Timecode	00	366 – 001	99 – 00	366 – 001	***2***
3.2.1	99	Freerun	N/A	000	99	000 – 001	
3.2.2	99	Freerun	N/A	364	99	364 – 365	
3.2.3	99	Freerun	N/A	365	99 – 00	365 – 000	
3.2.4	99	Freerun	N/A	366	99 – 00	366 – 000	
4.1.1	00	Timecode	N/A	000 – 001	00	000 – 001	
4.1.2	00	Timecode	00	365 – 366	00	365 – 366	***2***
4.1.3	00	Timecode	00	366 – 001	00 – 01	366 – 001	***2***
4.1.4	00	Timecode	99	365 – 001	00	365 – 001	***2***
4.2.1	00	Freerun	N/A	000	00	000 – 001	
4.2.2	00	Freerun	N/A	365	00	365 – 366	
4.2.3	00	Freerun	N/A	366	00 - 01	366 – 367	

Note 2: Day went to 000 for about one second, then went to day 001

1.5.2 TIME CODE

This function group provides access to functions controlling TFP card operation while decoding time code. These functions allow the user to control both the time code decoding and time code generating circuits of the device.

1.5.2.1 DECODE

This function allows the user to select the format and modulation types associated with an input timing signal. These values control how the device attempts to decode the input time code. These values may be set regardless of the mode but will only be used in time code decoding mode. The format defines the type of the time code data. The modulation defines the envelope for the signal and which input pin the signal will be extracted from. The default format is IRIG B and the default modulation envelope is AM (amplitude modulated).

1.5.2.2 GENERATE

This function allows the user to select the format of the time code that will be generated by the TFP device. The time code generator supports IRIG B and IRIG H DCLS.

1.5.3 SIGNALS

This group provides access to functions that control various hardware timing signals either decoded or generated by the TFP card.

1.5.3.1 HEARTBEAT (PERIODIC) OUTPUT

This function allows the user to command the TFP to produce a clock signal at a specified frequency. The heartbeat signal, also referred to as a periodic, can be either synchronous or asynchronous to the internal 1PPS epoch in the TFP device. This functionality is implemented in hardware on the TFP device by an Intel 82C54 counter timer chip. The heartbeat circuit has two 16 bit divisors, which are clocked by the counter. As the output of the first divisor provides the clock for the second divisor, manipulating the divisor values results in various duty cycles. The output of this circuitry is capable of creating a VME bus interrupt. See Section 4.1.5 for a description of how to program the heartbeat output.

1.5.3.2 STROBE OUTPUT

This function allows the user to command the TFP to produce a hardware signal at a particular time, or at a particular point during a 1 second interval. When major/minor mode is selected, a hardware signal will be produced when the internal time of the TFP device matches the values entered for the major and minor strobe registers. The major time in hours, minutes and seconds may be supplied in addition to the milliseconds loaded in the minor strobe register. When minor mode is selected, a strobe signal is produced every second when the internal millisecond count in the TFP device matches the value entered in the minor strobe register. The output of this circuitry is capable of creating a VME bus interrupt.

1.5.3.3 EVENT INPUT

This function allows the user to command the TFP device to monitor a hardware timing signal. The source for the signal can be either the External Event input on the device or the output of the Heartbeat (Periodic) mentioned earlier in this chapter. The External Event signal capture may be set to occur on either the rising or falling edge. The Heartbeat signal capture is always on the rising edge. When a signal occurs in the selected format, the time at which the signal occurred is loaded into the event time registers. The capture lockout checkbox can be used to control whether or not subsequent signals will overwrite the data in the event time registers. The output of this circuitry is capable of creating a VME bus interrupt.

1.5.3.4 FREQUENCY OUTPUT

This function allows the user to control the frequency signal output by the TFP device. The available frequencies are 1, 5 and 10 MHz. The default state of this output is 10MHz.

1.5.4 INTERRUPTS

This function allows the user to control the generation of VME bus interrupts by the TFP device. If the latch event time function is enabled, the TFP will latch the time in the event time registers when an interrupt is detected. The user may query the event time registers to see when a particular event occurred. The latch event time function should not be enabled when external events are selected as these already latch the time in the event registers. Three control registers are provided to control the VME interrupts.

1.5.5 OSCILLATOR PARAMETERS

This group allows the user to select an external oscillator or the on board oscillator, in addition to enabling/disabling disciplining and jamsyncing. If disciplining and jamsyncing are disabled, the oscillator control DAC can be programmed to hold the oscillator control voltage to a specific value. When the TFP is synchronized to an input time source, the oscillator will be disciplined to the input source signal.

1.5.6 SYNC RTC TIME TO EXTERNAL TIME

This function allows the user to force the Real Time Clock (RTC) time to the board time.

1.5.7 BOARD RESET

This function allows the user to reset the TFP device. This command is useful when starting a test or in the case that unexpected behavior is observed from the card. This function is not used during normal operation.

CHAPTER TWO

INSTALLATION AND SETUP

2.0 VME/VXI COMPATIBILITY SWITCHES

The TFP is designed for both VMEbus and VXIbus compatibility. Switches SW2-3 and SW2-4 are used to select the bus protocol. To select VXIbus compatibility set SW2-3 and SW2-4 to the OPEN or OFF position. To select VMEbus compatibility set SW2-3 and SW2-4 to the CLOSED or ON position.

SW1 and SW2 Location
Revision A Through Revision D

SW1 and SW2 Location
Revision H

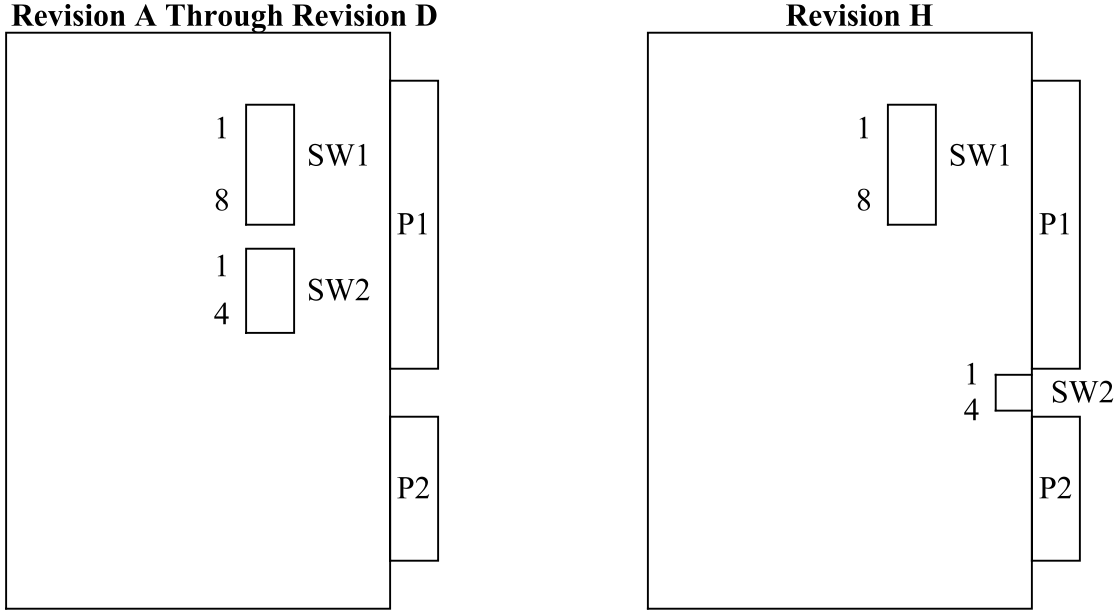


Figure 2-1 Address Switches

Switch SW2-3 controls the register block addressing within the A16 address space. With this switch in the VXI position, address bits A14 and A15 must be one for A16 selection. Switch SW1 is then used to select the logical address for the module. With SW2-3 in the VME position, the module can be mapped to any 64 byte block in the A16 address space. SW2-1 and SW2-2 set the A14 and A15 address bits, and SW1 is used to set the A13 through A6 address bits.

Switch SW2-4 controls the status/ID byte returned during interrupt acknowledge cycles. With SW2-4 in the VXI position, the Status/ID byte returned during interrupt acknowledge cycles is the logical address set with SW1. When SW2-4 is in the VME position, the Status/ID byte returned during interrupt acknowledge cycles is the user programmable vector loaded into the VECTOR register (discussed in Chapter Three).

2.1 VMEbus BASE ADDRESS SELECTION

Base address selection for the VMEbus requires the setting of switch SW1 (A6 through A13) and SW2 (A14 and A15). The bc635VME occupies 64 bytes in the A16 address space and can be freely located on any 64 byte boundary. The correspondence of the switch positions to the address bits is illustrated in Table 2-1.

Table 2-1
Address Bits Switch Positions

	SW2		**SW1**								
Address Bit	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	
Switch Number	2	1	8	7	6	5	4	3	2	1	A16 address range used. (The BASE address is on the left side.)
Example switch settings for SW1 and SW2.	0	0	0	0	0	0	0	0	0	0	0x0000 - 0x003F
1 = OPEN or OFF	0	0	0	0	0	0	0	0	0	1	0x0040 - 0x007F
0 = CLOSED or ON	0	0	0	0	0	0	0	0	1	0	0x0080 - 0x00BF
	0	0	0	0	0	0	0	0	1	1	0x00C0 - 0x00FF
	0	0	0	0	0	0	0	1	0	0	0x0100 - 0x013F
	…	…	…	…	…	…	…	…	…	…	…
	…	…	…	…	…	…	…	…	…	…	…
	1	1	1	1	1	1	1	0	1	1	0xEFC0 - 0xFEFF
	1	1	1	1	1	1	1	1	0	0	0xFF00 - 0xFF3F
	1	1	1	1	1	1	1	1	0	1	0xFF40 - 0xFF74

To select a base address, set each of the switches to the logical zero (CLOSED or ON) or the logical one (OPEN or OFF) state.

2.2 bc350VXI LOGICAL ADDRESS SELECTION

Logical address selection for the VXIbus requires the setting of switch SW1 (A6 through A13). The bc350VXI occupies 64 bytes in the A16 address space and can be located at any of the 256 logical addresses within the VXIbus. The correspondence between the switch positions and the address bits, and the logical state corresponding to a switch setting follows the description provided in Section 2.1

2.3 JUMPERS (DEFAULT SETTING IN BOLD TYPE)

The jumper locations for the Rev. A through Rev. F TFP versions are shown in Figure 2-2. The Rev. G and up along with the P100004 version jumpers are shown in Figure 2-3. The jumper blocks are not drawn to scale in order to make the numbers more visible. It may be helpful to refer to the schematic diagrams to obtain a clearer idea of the function of each jumper option.

JP1
With the jumper in the **1-2** position the TFP is configured to use DC level shift input timecode. In the 3-4 or open position the TFP is configured to use modulated timecode.

JP2 (GPS Option)
In the **1-2** position the TFP is configured to use a single ended 1pps GPS input. In the 3-4 position the TFP is configured to use a differential 1pps GPS input.

JP3 (GPS Option)
In the **1-2** position the TFP is configured to use the ACUTIME Smart Antenna or SV-6 as the GPS sensor. In the 3-4 position the TFP is configured to use the TANS as the GPS sensor. The ACUTIME, SV-6, and TANS are GPS sensor options that are available from Symmetricom, Inc. This jumper is not present on the P100004 model boards.

JP4
The jumpers in the JP4 group are designed to be moved as a pair. Positions 3-4 and 5-6 define one configuration, and positions 1-2 and 7-8 define a second configuration. In the default configuration the TFP is configured with an auxiliary RS-422 output. In the second configuration the TFP is configured in a daisy-chain mode (the RS-422 input is jumpered to the RS-422 output). This jumper set is intended to be used in a digital synchronization mode. At the present time this mode has not been implemented. This jumper is not present on the P100004 model boards.

JP5
In the 1-2 position this jumper places a “100Ω” load between the RS-422 input lines. In the **3-4** position the “100Ω” load is bypassed. When the TFP is the terminal device on an RS-422 daisy chain the load should be used. When the TFP is not at the end of the chain the load should be omitted.

JP6
In the **1-2** position this jumper places GROUND on P2 pin C12. In the 2-3 position the 1, 5, 10MHz clock is driven out of P2 pin C12. On the model P100004 boards, this jumper is implemented as a 2x2 pin block. A shunt on pins 2 and 4 enables the 10MHz output on P2 pin C12. A shunt on pins **1 and 2** disables the output by grounding P2 pin C12.

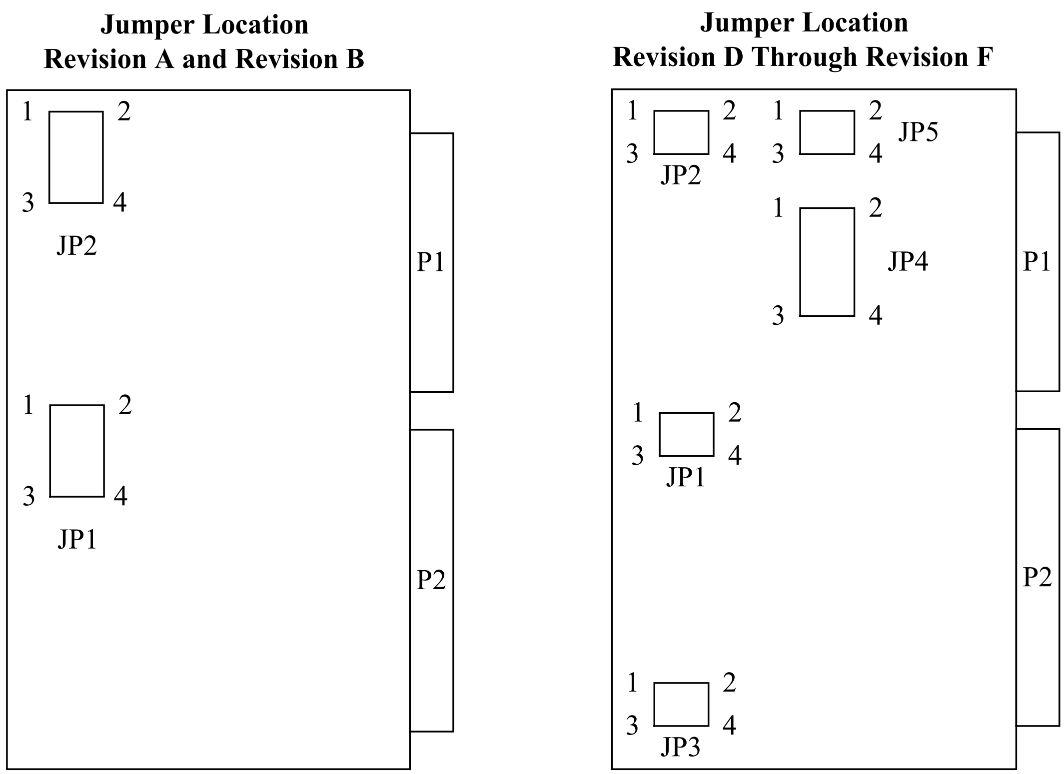


Figure 2-2 Jumper Locations I

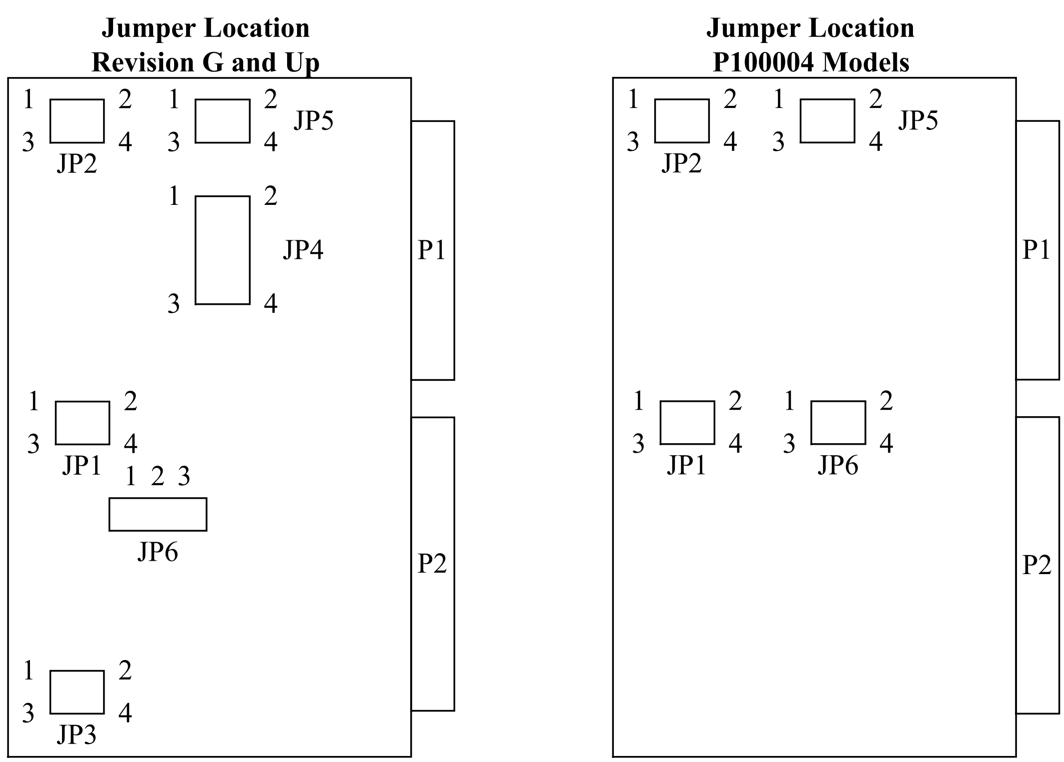


Figure 2-3 Jumper Locations II

2.4 INSTALLATION

To install the TFP into a computer chassis follow the steps below.

- Remove the IACKIN*/IACKOUT* back plane jumper for the TFP slot. This step should be performed even if TFP interrupts are not used.

- bc635VME users must verify that signals on rows A and C of the P2 connector are not used for VSB or other purposes. The TFP provides signal I/O on rows A and C that may produce a conflict. If a conflict does exist, a solution is to obtain a bc635VME with the P2 connector removed.

- Verify that power is off and insert the TFP into the chassis, securing it in the slot by tightening the two front panel screws.

This Page Intentionally Left Blank.

CHAPTER THREE
INTERFACES

3.0 GENERAL

The TFP occupies 64 bytes in the VMEbus/VXIbus, A16 address space. Refer to Section 2.1 for details on VMEbus Base Address selection, and to Section 2.2 for VXIbus logical address selection. TFP data transfers are D16 with the exception of packet I/O which allows D08(0) transfers. A glossary of key terms commonly used in the discussion of timing operation is provided below.

Epoch
A reference time or event. Epoch often refers to a one pulse per second event.

Flywheel
Maintain time or frequency accuracy as well as local resources when a time or frequency reference has been lost or removed.

Periodic
A programmable frequency which is obtained by dividing the TFP reference frequency. Periodics are sometimes referred to as "heartbeats." Periodics may optionally be synchronous with the 1pps epoch if the period is expressible as a ratio of integers.

Major Time
Units of time larger than or equal to seconds. A *day hr:min:sec* format is usually implied.

Minor Time
Subsecond time to whatever resolution is supported.

Packet
A group of bytes conforming to a defined structure. Packets are usually used in bit serial or byte serial data transmission to allow framing of the transmitted data.

3.1 DATA INPUT AND OUTPUT

Communication with the TFP is performed using a set of memory mapped registers. These registers may be read only (R), write only (W), or read/write (R/W). In some cases a read/write register is structured to support dissimilar data in the read and write directions. Table 3-1 summarizes the type of register located at each hexadecimal offset, and provides a brief description of the register function. The data format and detailed descriptions of each register are provided in the next section.

Table 3-1

TFP Register Map Summary			
HEX Offset	**Type**	**Label**	**Function Read/Write**
0	R	ID Register.	VXIbus ID Register
2	R	Device.	VXIbus Device Type Register
4	R/W	Status/Control.	VXIbus Status / Control Registers
6-08	Reserved		
0A	R	TIMEREQ	Time Request (Time Latching Strobe)
0C	R	TIME0	Requested Time (includes status byte)
0E	R	TIME1	Requested Time
10	R	TIME2	Requested Time
12	R	TIME3	Requested Time
14	R	TIME4	Requested Time
16	R	EVENT0	Event Time
18	R/W	EVENT1 / STROBE1	Event Time/Strobe Time
1A	R/W	EVENT2 / STROBE2	Event Time/Strobe Time
1C	R/W	EVENT3 / STROBE3	Event Time/Strobe Time
1E	R	EVENT4	Event Time
20	R/W	UNLOCK	Release Lockout/Capture Time
22	R/W	ACK	Acknowledge Register
24	R/W	CMD	Command Register
26	R/W	FIFO	FIFO Input/Output (D16 or D08[O])
28	R/W	MASK	Interrupt Mask
2A	R/W	INTSTAT	Interrupt Status
2C	R/W	VECTOR	Interrupt Vector
2E	R/W	LEVEL	Interrupt Level
30-3E	Reserved		

Offset 0x00 ID REGISTER Reset Value 0xXef4

This register was implemented to satisfy the VXIbus Specification. Bit assignments are as follows.

Table 3-2

Bit #	**15-14**	**13-12**	**11-0**
Use Of Field	Device Class	Addressing Modes	Manufacturer's ID
TFP Meaning	Register Based *	A16 Only *	0xef4

* Bits 12-15 are not driven high during a read of the ID Register. In most cases they will float high during a read cycle.

Offset 0x02 DEVICE Reset Value 0xX350
This register simply contains (in the case of an A16 only device) a manufacturer's card ID. Bits 12-15 are not driven high during a read of the Device Register. In most cases they will float high during a read cycle.

Offset 0x04 STATUS Reset Value 0xffff
The TFP does not support VXIbus initialization and diagnostic features. The reset value is always returned.

Offset 0x04 CONTROL Reset Value 0xfffe
Writing to this register with bit 0 set will deassert any pending interrupts and will clear all used bits in offsets 0x20 through 0x2E (except FIFO at offset 0x28). Writing to this register with bit zero cleared has no effect. All other bits are ignored during a write.

Offset 0x0A TIMEREQ Reset Value NA
Reading this register latches the current time and status into offsets 0x0C through 0x14. The value read is indeterminate.

*** * * WARNING * * ***

Many compilers will optimize out of existence an assignment made to a local variable if that variable is not used. For example, the following code snippet may not read offset 0x0A.

```
timeptr = (short *)(BASE + 0x0A) ;          /* initialize pointer */
local_dummy = *timeptr++ ;                  /* latch the time ?? */
read_time(timeptr) ;                        /* read the time */
```

The following form is recommended. Use of the global prevents optimizing out.

```
timeptr = (short *) (BASE + 0x0A) ;         /* initialize pointer */
global_dummy = *timeptr++ ;                 /* latch the time */
read_time(timeptr) ;                        /* read the time */
```

Offset 0X0C	**TIME0**	**Reset Value NA**
Offset 0X0E	**TIME1**	**Reset Value NA**
Offset 0X10	**TIME2**	**Reset Value NA**
Offset 0X12	**TIME3**	**Reset Value NA**
Offset 0X14	**TIME4**	**Reset Value NA**

For clarity the above offsets have been grouped.

Table 3-3

Bit #	15-12	11-8	7-4	3-0
TIME0 Field	Not Defined	Not Defined	Status (Note 1)	Days Hundreds
TIME1 Field	Days Tens	Days Units	Hours Tens	Hours Units
TIME2 Field	Minutes Tens	Minutes Units	Seconds Tens	Seconds Units
TIME3 Field	10E-1 Seconds	10E-2 Seconds	10E-3 Seconds	10E-4 Seconds
TIME4 Field	10E-5 Seconds	10E-6 Seconds	10E-7 Seconds	Not Defined

Offset 0x16 EVENT0 Reset Value NA
Offset 0x18 EVENT1 Reset Value NA
Offset 0x1A EVENT2 Reset Value NA
Offset 0x1C EVENT3 Reset Value NA
Offset 0x1E EVENT4 Reset Value NA

For clarity the above offsets have been grouped.

Table 3-4

Bit #	15-12	11-8	7-4	3-0
EVENT0 Field	Not Defined	Not Defined	Status (Note 1)	Days Hundreds
EVENT1 Field	Days Tens	Days Units	Hours Tens	Hours Units
EVENT2 Field	Minutes Tens	Minutes Units	Seconds Tens	Seconds Units
EVENT3 Field	10E-1 Seconds	10E-2 Seconds	10E-3 Seconds	10E-4 Seconds
EVENT4 Field	10E-5 Seconds	10E-6 Seconds	10E-7 Seconds	Not Defined

***Note*:**	bit 6	1 = frequency offset > 5E7 in Mode 0	0 = frequency offset < 5E7 in Mode 0
		1 = frequency offset > 5E8	0 = frequency offset < 5E8
	bit 5	1 = time offset > X microseconds	0 = time offset < X microseconds
		(X = 5 for mode 0	X = 2 more all other modes)
	bit 4	1 = flywheeling (not locked)	0 = locked to selected reference

Offset 0x18 STROBE1 Reset Value 0xXX00
Offset 0x1A STROBE2 Reset Value 0x0000
Offset 0x1C STROBE3 Reset Value 0x0000

For clarity the above offsets have been grouped.

Table 3-5

Bit #	15-12	11-8	7-4	3-0
STROBE1 Field	Not Defined	Not Defined	Hours Tens	Hours Units
STROBE2 Field	Minutes Tens	Minutes Units	Seconds Tens	Seconds Units
STROBE3 Field	10E-1 Seconds	10E-2 Seconds	10E-3 Seconds	Not Defined

Offset 0x20 UNLOCK Reset Value NA

A read of this register releases the time capture lockout function if it has been enabled. See "CMD OFFSET 0x24" for additional details. The data read from this offset is meaningless. A write to the UNLOCK register acts as a secondary time latching strobe. Time is latched in EVENT0 - EVENT4. This feature allows the host to capture two times independently.

Offset 0x22 ACK Reset Value 0xXX00

Table 3-6

Bit #	Control	Function (SET = "1" = High Voltage, CLEAR = "0" = Low Voltage)
0	TFP HOST	SETS bit to acknowledge the receipt of a valid input packet from host CLEARS bit by writing to this register with bit 0 SET.
1	Reserved	
2	TFP HOST	SETS bit when output FIFO contains a data packet. CLEARS bit by writing to this register with bit 2 SET. This bit can generate an interrupt. (see OFFSET 0x2A INTSTAT).
3	Reserved	
4	TFP HOST	SETS bit if output FIFO contains data. CLEARS bit if output FIFO empty. CLEARS output FIFO by writing to this register with bit four SET.
5	Reserved	
6	Reserved	
7	HOST	*Must* write to this register with bit seven SET to cause TFP to take action on the data packet previously written to the input FIFO.
8-15	Reserved	

Offset 0x24 CMD Reset Value 0xXX00

This register is used to command the TFP to perform specific functions.

Table 3-7

<table>
<tr><th>Bit #</th><th>Name</th><th colspan="8">Function</th></tr>
<tr><td>0</td><td>LOCKEN</td><td colspan="8">Event capture lockout (0 = disable lockout 1 = enable lockout).
Prevents a new event from overwriting a previous event until an UNLOCK is performed (see OFFSET 0x20 UNLOCK).</td></tr>
<tr><td>1</td><td>HBEN</td><td colspan="8">Enable periodic time capture (0 = disable 1 = enable).
When enabled the periodic output is logically OR'ED with the event input, and the time of the periodic may be read in EVENT0 - EVENT4.</td></tr>
<tr><td>2</td><td>EVSENSE</td><td colspan="8">Event capture sense select (0 = rising edge 1= falling edge).</td></tr>
<tr><td>3</td><td>EVENTEN</td><td colspan="8">Event capture enable (0 = disable 1 = enable).</td></tr>
<tr><td>4</td><td>STREN</td><td colspan="8">Time coincidence output strobe enable (0 = disable 1 = enable).</td></tr>
<tr><td>5</td><td>STRMODE</td><td colspan="8">Strobe mode (0 = use major and minor time 1 = use minor time only).
In mode (1) an output strobe is produced each second.</td></tr>
<tr><td>6</td><td>FREQSEL0</td><td>0</td><td rowspan="2">10 MHz</td><td>1</td><td rowspan="2">5 MHz</td><td>0</td><td rowspan="2">1 MHz</td><td>1</td><td rowspan="2">1 MHz</td></tr>
<tr><td>7</td><td>FREQSEL1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>8-15</td><td colspan="9">Reserved</td></tr>
</table>

Offset 0x26 FIFO Reset Value NA

Reads take data from the output FIFO. Writes place data into the input FIFO. Both the input FIFO and the output FIFO may also be accessed via D08(O) at offset 0x27. Each FIFO has a depth of 512 bytes.

Data must be written to and read from the FIFO in the following data packet format.

byte 1	0x01	header byte (ASCII SOH)
byte 2	"A" through "Z"	idbyte (defined in Chapter Four)
byte 3	data	always ASCII i.e. 0 = 0x30
byte 4	data	
.	.	the number of data bytes varies
byte N	data	
byte N+1	0x17	tail byte (ASCII ETB)

Offset 0x28 MASK Reset Value 0xXX00

Table 3-8

Bit #	INT #	Source Of Interrupt
0	0	External event input has occurred.
1	1	Periodic pulse output has occurred.
2	2	Time coincidence strobe has occurred.
3	3	The one pulse per second (1pps) output has occurred.
4	4	A data packet is available in the output *FIFO*.
5-15	Reserved	

An interrupt source is enabled by writing a one to the mask bit corresponding to that source. An interrupt source is disabled by writing a zero to the mask bit corresponding to that source.

Offset 0x2A INTSTAT Reset Value 0xXX00

The INTSTAT register has the same basic structure as the MASK register. The TFP sets bits zero through four of this register depending upon which interrupt source generated the interrupt. The INTSTAT register bits are set regardless of the state of the mask bits. This feature allows the host to poll for the occurrence of the interrupt sources. INTSTAT bits are cleared by writing to the INTSTAT register with the corresponding bit(s) set.

*** * * WARNING * * ***

It is the transition of an INTSTAT bit from a zero to a one that causes an interrupt to be generated (assuming that the corresponding MASK bit was set). If the bit in the INTSTAT register is not cleared by the host it is not possible to generate a second interrupt. It is good programming practice to clear the INTSTAT register immediately after interrupts have been enabled.

Offset 0x2C VECTOR Reset Value 0xXX00

The VECTOR register holds the eight bit Status/ID byte that the TFP will return during interrupt acknowledge cycles for VMEbus applications.

Offset 0x2E LEVEL Reset Value 0xXX00

The LEVEL register selects the level at which an interrupt will be generated. Only bits zero through two are used. These bits are encoded as follows:

Bit			**IRQ Level**
0	0	0	Disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

CHAPTER FOUR

FIFO DATA PACKETS

4.0 GENERAL

Communication with the TFP is performed using a byte serial data packet protocol. The packet bytes are read from, and written to the TFP, using D08(O) transfers at offset 0x27 or D16 transfers at offset 0x26. In the case of a D16 transfer, only the low order byte is used. The packet structure is defined in Chapter Three, "OFFSET 0x26."

4.1 WRITING DATA PACKETS

The following steps should be followed when loading data packets to the TFP. Failure to perform one or more of these steps correctly is a common reason for customer support calls.

- Write the packet to the input FIFO.
- Clear bit 0 of the ACK register by writing 0x01 to the ACK register.
- Inform the TFP that an input packet is available by writing 0x80 to the ACK register.
- The TFP will set bit 0 of the ACK register when the packet is processed.

When the host sets bit seven of the ACK register an interrupt to the TFP CPU is generated. The TFP service routine performs minimalist packet integrity checking. The TFP checks that the first packet byte is 0x01 (ASCII SOH). If the SOH is found, the TFP loads FIFO data into an input buffer until a byte value of 0x17 (ASCII ETB) is found. The packet is then processed in accordance with the idbyte value. When processing is complete, the TFP sets bit zero of the ACK register, clears the input FIFO, and resumes its previous task. If an SOH is not the first packet byte, if more than 40 bytes are read before encountering an ETB, or if the idbyte value is invalid, then TFP clears the FIFO, clears bit zero of the ACK register, and resumes its previous task.

4.1.1 PACKET "A" SELECT TFP OPERATIONAL MODE

This packet contains a single data byte (zero through seven) which defines the TFP operational mode. The mode is saved in the battery backed RAM. The modes are enumerated below.

Mode 0 (Zero) Time Code Decoding Mode
The TFP uses an input timecode as the timing reference. See packet "H" for time codes supported. Both modulated carrier and DC level shift formats are supported (DC level shift is not supported for 2137 or XR3 codes). The TFP locks its crystal oscillator to the input code rate. The oscillator has a control range of ±30PPM for the standard DPI version, and ±2PPM for the optional oven version. If the input code is outside these limits, the TPF will exhibit periodic slips (if the TFP reference deviates from the input source by more than ± 1 millisecond, a forced jamsync is performed). If the input code is lost or removed, the TFP will continue to "flywheel" at the last known code rate. Typical accuracy is five parts in 10^7 (two milliseconds of drift per hour).

Mode 1 Free Running Mode
This mode is virtually the same as Mode 2. Without a 1pps input the TFP runs at the last known oscillator frequency. Major time can be set with the "B" packet. The TFP timebase can be adjusted with packet "D."

Mode 2 External 1 pps Mode
The TFP synchronizes to the signal on the 1pps input. Major time can be loaded with the "B" packet. The acquisition range is the same as described in mode zero.

Mode 3 Real Time Clock Mode
The TFP synchronizes to the onboard real time clock (RTC) IC, and the major time is also derived from the clock IC. The RTC is battery backed. This mode is not recommended when using the oven oscillator because the accuracy of the RTC is not high enough to ensure that the oven will be able to track it with slippages. See Mode 0 (zero) description.

Mode 4 Digital Sync Mode
This mode is not implemented.

Mode 5 GPS Mode with GPS Receiver Onboard (Obsolete)
The TFP only supports this mode in the bc635VME/bc357VXI configuration. It is currently available only in a double wide 6U form factor.

Mode 6 GPS Mode with GPS Receiver Located in the Antenna
This is an optional mode available with the bc637VME/bc357VXI configuration. It is described in a separate User's Guide.

Mode 7 Diagnostic and Default Setting Mode
Initially this mode was provided to allow the TFP to be photographed. The LED display is loaded with static time 12:34:56. As more battery backed parameters were added it became useful to use this mode as a means of setting all battery backed data to standard defaults. This data and the default values established by mode seven are as follows, see Table 4-1.

Table 4-1
Mode 7 Default Values

Variable	Default	Description
Mode	See Note	TFP Operational Mode
Time Code	IRIG B	Reference Time Code Expected
Format	Modulated	Modulated Time Code Expected
Gencode	IRIG B	TFP Generates IRIG B
Path	1	Path Selection Variable (See "P" Packet)
Local	0	Local Time Offset (GPS Modes Only)
Accum	32000	VCXO DAC Value (Nominally Centered)
Leapsec	0	GPS To UTC Leap Second Correction (Only Used In GPS Modes)

The diagnostic utility of this mode resides in the fact that the operator can immediately determine if the host program is communicating properly with the TFP by simply observing the display. To borrow from the classic K&R, to make 12:34:56 appear "you have to be able to create the program text, compile it, run it, and find out where your output went. With these mechanical details mastered, everything else is comparatively easy."

Note: The bc635 defaults to Mode 0 (zero). The bc637 defaults to Mode 6.

4.1.2 PACKET "B" SET MAJOR TIME

In Mode 1 and Mode 2 the only way to set major time is using this packet. It is not likely that this packet would be used in any other mode since all other modes derive major time from the timing reference signal. The packet format is as follows:

byte	1	SOH
byte	2	"B"
byte	3	days hundreds
byte	4	days tens
byte	5	*days units (Jan 1 is defined as day 001)
byte	6	hours tens
byte	7	hours units
byte	8	minutes tens
byte	9	minutes units
byte	10	seconds tens
byte	11	seconds units
byte	12	ETB

Note: All data fields must be in ASCII format.

*Day 000 is an invalid time code in IRIG time codes. If Day 000 is desired, see "Packet 'P' Path Selection."

The time loaded by packet "B" will not be used until the one second epoch following the load. The TFP increments the time before loading it to output buffer registers. The time is incremented at approximately 918 milliseconds into the current frame, and the buffer registers are loaded 950 milliseconds into the current frame. The buffer registers are transferred to a set of holding registers synchronously with the 1pps output. The time loaded by packet "B" should be input well in advance of the 918 millisecond point in the frame, and should reference the current frame.

4.1.3 PACKET "C" COMMAND INPUT

This packet has a single data byte and is used to direct the TPF to take the specific actions below.

byte	1	SOH	
byte	2	"C"	
byte	3	"1" - "6"	(Definitions Below)
byte	7	ETB	

"1"	Not Used	(Warm Start on Early Software Versions)
"2"	Software Reset	vectors TFP CPU to Power on Reset Point
"3"	Jamsynch	Force TFP Minor Time To Zero on the Next 1pps Input
"4"	Not Used	(Jamsynch Lockout On Early Software Versions)
"5"	Buf to RTC	Load Current Time to the Real Time Clock IC
"6"	Variables	Dumps Battery Backed RAM to FIFO (Factory Use Only)

4.1.4 PACKET "D" LOAD D/A CONVERTER

The TFP reference crystal oscillator is voltage controlled using the buffered output of a 16 bit D/A converter as the controlling voltage. Packet "D" allows the user to directly load a 16 bit value to the D/A converter. This feature would allow a user to fine tune the TFP time base in the free running mode. We are not aware of any other use for this packet in normal operation. Since this voltage is routed out of the TFP via pin 9 on the J1 connector to allow external oscillators to be disciplined, it would provide a means to devise a frequency control algorithm independent of the TFP. The format is shown below. (See also bit 3 of the path byte loaded by the "P" packet.)

byte	1	SOH	
byte	2	"D"	
byte	3	"0" - "F"	bits 12-15
byte	4	"0" - "F"	bits 08-11
byte	5	"0" - "F"	bits 04-07
byte	6	"0" - "F"	bits 01-03
byte	7	ETB	

Note: All data fields must be in ASCII format.

4.1.5 PACKET "F" HEARTBEAT (PERIODIC) CONTROL

This packet establishes the frequency of the TFP output periodics. The number of output pulses is defined by the following equation.

N = 10,000,000 / (n1 * n2)

where N = output pulses per second
n1 = a programmable number in the range of 2 to 65535
n2 = a programmable number in the range of 2 to 65535

The "F" packet establishes the value of n1 and n2. There is a one byte qualifier associated with the "F" packet. This qualifier allows the periodics to be asynchronous or synchronous with respect to the 1pps epoch. If the synchronous format is chosen n1 and n2 must be selected such that N is an integer.

The duty cycle of the output waveform is dependent on the particular values of n1 and n2 selected. Divider n2 physically follows divider n1. The following example serves as an illustration. If n1 * n2 = 20, the output frequency is 500kHz. If n1 is selected as ten and n2 is selected as two a square wave is output since the last divider is a divide by two. If n1 is selected as two and n2 is selected as ten the output waveform is a pulse train with a one tenth duty cycle.

The packet "F" format is as follows:

byte	1	SOH
byte	2	"F"
byte	3	"2" for asynchronous "5" for synchronous
byte	4	"0" - "F" m1 bits 12-15
byte	5	"0" - "F" m1 bits 08-11
byte	6	"0" - "F" m1 bits 04-07
byte	7	"0" - "F" m1 bits 00-03
byte	8	"0" - "F" m2 bits 12-15
byte	9	"0" - "F" m2 bits 08-11
byte	10	"0" - "F" m2 bits 04-07
byte	11	"0" - "F" m2 bits 00-03
byte	12	ETB

If a two (asynchronous) qualifier is used then the values of n1 and n2 are the same as the packet values m1 and m2. If the five (synchronous) qualifier is used, then the values of n1 and n2 are equal of packet values m1+1 and m2+1 respectively. For example, if a synchronous 500KHz square wave is desired then the qualifier byte is five, m1 = 9, and m2 = 1. Additional insight into the operation of the counter can be gained by reading the Intel documentation for the 82C54 integrated circuit. The two and five qualifiers correspond to the Intel defined Modes 2 and 5.

The periodic engine of the bc635/637VME consists of two sections of an INTEL 82C54 programmable interval timer connected in a serial configuration and driven by the TFP 10 MHz reference. Glue logic in one of the logic cell arrays supports both synchronous (with the 1pps epoch) and asynchronous operation. It is helpful (although not essential) to read the INTEL data sheet on the 82C54. Packet "F" allows the user complete access to the serial counters using standard INTEL loading protocols.

Two counter modes are supported; 1pps synchronous and asynchronous. It is the responsibility of the user to select the appropriate mode. No error checking is performed by the bc635/637VME firmware. The synchronous mode should only be selected if the number of output counts per second is an integer. If the number of counts per second is not an integer then the asynchronous mode should be used. The number of counts per second is always of the following form:

N = (10,000,000) / (n1 * n2)

where: N = counts per second
n1 = Counter #1 divide
n2 = Counter #2 divide

The range of values for Counter #1 and #2 is mode dependent as follows.

Asynchronous Mode: 2 to 65535
Synchronous Mode: 3 to 65535

* * * WARNING * * *

Periodic heartbeat pulse/interrupt generation can not be guaranteed in synchronous mode when counter divide values of two are used.

The two modes of operation are accessed using standard INTEL mode identifiers. For synchronous operation the mode byte must be an ASCII "5." For asynchronous operation the mode byte must be an ASCII "2." The packet format is as follows:

byte	1	SOH.
byte	2	"F."
byte	3	ASCII "2" (asynch) or "5" (synch).
byte	4	ASCII "0" - "F" (n1 bits 2-15).
byte	5	ASCII "0" - "F" (n1 bits 8-11).
byte	6	ASCII "0" - "F" (n1 bits 4-7).
byte	7	ASCII "0" - "F" (n1 bits 0-3).
byte	8	ASCII "0" - "F" (n2 bits 12-15).
byte	9	ASCII "0" - "F" (n2 bits 8-11).
byte	10	ASCII "0" - "F" (n2 bits 4-7).
byte	11	ASCII "0" - "F" (n2 bits 0-3).
byte	12	ETB.

* * * IMPORTANT * * *

When Mode 5 is used, the value of n1 and n2 produced by the 82C54 hardware is n1+1 and n2+1. This is a result of the way INTEL designed the 82C54, and is unrelated to our design.

Example: It is desired to implement 10000 counts per second synchronous with the 1pps.

mode = "5" (synchronous)
n1+1 = 10
n2+1 = 100 (10,000,000) / (10 * 100) = 10000

byte	1	SOH.
byte	2	"F."
byte	3	"5" (mode).
byte	4	"0."
byte	5	"0."
byte	6	"0."
byte	7	"9" (n1 = 9).
byte	8	"0."
byte	9	"0."
byte	10	"6."
byte	11	"3" (n2 = 99 = 0x63).
byte	12	ETB.

Other values of (n1+1) and (n2+1) could have been used. For example, (n1+1) = 25 and (n2+1) = 40.

4.1.6 PACKET "G" PROPOGATION OFFSET CONTROL

It is frequently desired to program an offset into the basic TFP timekeeping functions relative to the reference input. For example, if the reference input is an IRIG B timecode, there may be significant cable delay between the IRIG B generator and the TFP location. Packet "G" allows this time difference to be removed by inserting the known amount of offset between the IRIG B reference and TFP locations. The offset is programmable in units of one hundred nanoseconds, and may be positive or negative. The format is shown below.

byte	1	SOH	
byte	2	"G"	
byte	3	"+" or "-" advance or retard	
byte	4	"0" - "9"	BCD millisecond hundreds
byte	5	"0" - "9"	BCD millisecond tens
byte	6	"0" - "9"	BCD millisecond units
byte	7	"0" - "9"	BCD microsecond hundreds
byte	8	"0" - "9"	BCD microsecond tens
byte	9	"0" - "9"	BCD microsecond units
byte	10	"0" - "9"	BCD nanosecond hundreds
byte	11	ETB	

For the IRIG B scenario described above, a positive offset should be used.

*** * * WARNING * * ***

If offsets larger than ± 990 microseconds are used, then the TFP jamsynch feature must be turned off using packet "P." The reason for this requirement is that under normal operation if a difference between the reference time and the TFP time is detected to be greater than ±1 millisecond the TFP timbers is "jammed" to the reference time so that a lengthy steering process is avoided.

4.1.7 PACKET "H" SET TIMECODE FORMAT FOR MODE 0

Packet "H" allows the host to select the timecode format and modulation type. The packet format is as follows. The timecode format and modulation values are maintained in battery backed RAM.

byte	1	SOH
byte	2	"H"
byte	3	format
byte	4	modulation
byte	5	ETB

Format Choices

"A"	IRIG A
"B"	IRIG B
"C"	2137 (XR3 with 100Hz symbol rate)
"N"	NASA 36
"X"	XR3 (25Hz symbol rate)

Modulation Choices

"M"	amplitude modulated sine wave Modulated not supported for IRIG A
"D"	pulse code modulation (DC level shift) DC level shift not is supported for 2137 and XR3 codes.

4.1.8 PACKET "I" CLOCK SOURCE SELECT

Packet "I" is used to select the clock source for the TFP. The TFP uses a frequency of 10MHz for all timing functions. The 10 MHz be may derived from the TFP VCXO or it may be supplied from an external oscillator via J1 pin #1 or P2 pin #C22. The packet format is as follows.

byte	1	SOH
byte	2	"I"
byte	3	"E" or "I" External or Internal
byte	4	ETB

On power on the TFP always defaults to the internal oscillator selection. This packet has no effect on boards with Oven Oscillators

4.1.9 PACKET "J" SEND DATA TO GPS RECEIVER

The format and content variations are discussed in a separate User's Guide.

4.1.10 PACKET "K" SELECT GENERATOR CODE

The timecode generated by the TFP is selected by packet "K." Only two options are available as described below. The generator code type is maintained in battery backed RAM.

byte	1	SOH
byte	2	"K"
byte	3	code
byte	4	ETB

Code Options

"B" generate IRIG B amplitude modulated and DC level shift
"H" generate IRIG H DC level shift only

4.1.11 PACKET "L" SET REAL TIME CLOCK

This packet loads the battery backed real time clock IC which is used as the source of major time and 1pps epoch when mode three is selected. The format is shown below.

byte	1	SOH
byte	2	"L"
byte	3	years tens
byte	4	years units
byte	5	months tens
byte	6	months units (January = month 1)
byte	7	day-of-month tens
byte	8	day-of-month units
byte	9	hours tens
byte	10	hours units
byte	11	minutes tens
byte	12	minutes units
byte	13	seconds tens
byte	14	seconds units
byte	15	ETB

All data fields must be in ASCII format. The TFP need not be in mode three when packet "L" is downloaded.

4.1.12 PACKET "M" LOCAL TIME OFFSET SELECT (GPS MODES ONLY)

This packet allows time to be displayed with a hour offset. This situation usually arises when the source of time is in an UTC (Universal Time Coordinated) format and the local time is desired to be displayed. The offset only applies to the hour's digits. This offset is maintained in battery backed RAM. The format is as follows.

byte	1	SOH	
byte	2	"M"	
byte	3	sign	"+" or "-"
byte	4	hours tens	
byte	5	hours units	
byte	6	ETB	

The hours are in range, from -12 to +12. A positive sign is used from the prime meridian heading East, and a negative sign is used from the prime meridian heading West. For example, Eastern Standard Time would be -05 relative to UTC.

4.1.13 PACKET "O" REQUEST DATA FROM THE TFP

This packet is used to request data from the TFP which is not available via the register interfaces. It was added as a "catch all" packet for universal data transfer. This packet has been created with a very extensive format, and additional data will be made available as customer needs and suggestions are addressed. The primary purpose of this packet is to allow the user to verify the integrity of the programmed setup data.

Note: The user is advised that repetitively issuing Packet "O" can cause excessive CPU overhead and may disrupt time keeping.

Currently three different data packets may be requested using the "O" packet. The formats are as follows:

Request Format

byte	1	SOH
byte	2	"O"
byte	3	"0" or "1" or "2" ...
byte	4	ETB

Response Format "0" Request RTC Time (See Packet "L")

byte	1	SOH
byte	2	"o" (lower case letter)
byte	3	"0" (zero)
byte	4	years tens
byte	5	years units
byte	6	months tens
byte	7	months units
byte	8	day-of-month tens
byte	9	day-of-month units
byte	10	hours tens
byte	11	hours units
byte	12	minutes tens
byte	13	minutes units
byte	14	seconds tens
byte	15	seconds units
byte	16	ETB

Response Format "1" Request Current D To A Value

byte	1	SOH	
byte	2	"o"	(lower case letter)
byte	3	"1"	
byte	4	"0" - "F"	bits 12-15
byte	5	"0" - "F"	bits 08-11
byte	6	"0" - "F"	bits 04-07
byte	7	"0" - "F"	bits 00-03
byte	8	ETB	

Response Format "2" Request Leap Seconds (Currently GPS Specific)

byte	1	SOH	
byte	2	"o"	(lower case letter)
byte	3	"2"	
byte	4	leap second tens	
byte	5	leap second units	
byte	6	ETB	

Response Format "3" Request RTC Year

byte	1	SOH
byte	2	"o" (lower case letter)
byte	3	"3"
byte	4	RTC years tens
byte	5	RTC year units
byte	6	ETB

Response Format "4" Request Year

byte	1	SOH
byte	2	"o" (lower case letter)
byte	3	"4"
byte	4	years tens
byte	5	year units
byte	6	ETB

The TFP signals a packet ready condition by setting bit 2 in the ACK register. It is the responsibility of the host to clear this bit by writing to the ACK register with bit 2 set.

4.1.14 PACKET "P" PATH SELECTION

The path selection might better be called a switch or branch selector. The purpose of this packet is to allow the user to exercise control over certain TFP processes. The path packet is used to download a single byte. Each bit in the byte has a toggling action relative to a TFP function. The format is described below.

byte	1	SOH
byte	2	"P"
byte	3	"0" - "F" path upper nibble
byte	4	"0" - "F" path lower nibble
byte	5	ETB

Upper Nibble Bit Definitions

bit	3	0 = normal time format	1 = long second format (See Note.)
bit	2	0 = no broadcast of RTC	1 = broadcast packet "o" "0" each second
bit	1	0 = use GPS leap seconds	1 = ignore GPS leap seconds
bit	0	0 = FIFO echo off	1 = FIFO echo on

Lower Nibble Definitions

bit	3	0 = enable TFP disciplining	1 = disable TFP discipline
bit	2	0 = enable jamsynch	1 = disable jamsynch
bit	1	0 = leap year off	1 = leap year on
bit	0	0 = Accept Day 000	1 = Day 000 invalid (default setting)

Note: Time∅ through TIME4 contain atomic seconds since January 6, 1980. Use only in GPS Mode. (See Table 4-2.)

4.1.14.1 LOWER NIBBLE BIT DESCRIPTIONS

Bit 0

In Time Code mode (Mode 0) it is sometimes desired to use day 000. This is an invalid code in IRIG time codes and clearing this bit overrides the normal checking and allows a board lock on this otherwise invalid code. See Chapter Three for a description of the TIME fields (offset 0x0C).

Note: Day 001 is always January 1 as per IRIG specifications. We allow day 000 only for those people that want this capability, say for testing purposes (many time-code generators start with Day 000), and are not bothered by an extra day in the year roll over.

Bit 1
During leap years this path bit must be set to enable the different day counts which represent leap years.

Note: Software versions later than 9501128 use the "S" packet to set the year and then calculates the leap year. In this software the leap year bit has no effect.

Bit 2
Jamsynch is a method employed to match the output 1pps signal to the input time mark. If you change modes of operation on a warmed up unit and want to rush the re-synchronizing you can enable jamsynch, then use Packet "C" to force a jamsynch of the unit, which will cause the 1pps signal to be reset to the time-mark time. There are disadvantages to using this method. If a strobe was scheduled for a time between the flywheeling time and the jamsynch it will be missed in the jump to the new time. There is also a break in the lock for a couple of seconds. Jamsynchs are ineffective on a cold unit that has the oscillator changing frequency at a high rate during warm up.

Bit 3
Oscillator disciplining might be disabled if you were using an external clock source that requires a different disciplining routine and you are using the on-board DAC and disciplining through a Packet "D."

4.1.14.2 UPPER NIBBLE BIT DESCRIPTIONS

Bit 0
When enabled, packets written to the INPUT FIFO will be automatically echoed to the OUTPUT FIFO.

Bit 1
This bit is used when you want to report UTC time instead of GPS time. The change is that leap seconds are added to the time to derive UTC.

Bit 2
When enabled, the RTC data is automatically inserted into the OUT-FIFO every second. This could be useful if you have a system that is maintaining two different times such as UTC and local time.

Bit 3
In GPS mode (Mode 5 or 6) you may want to report the time in seconds from the start of the GPS epoch (seconds from start of January 6, 1980). Some systems may find it easier to deal with time strictly in seconds. The table below reflects that fields TIME1 and TIME2 contain a 32 bit contiguous binary number representing GPS Epoch seconds. The minor time remains in decimal sub-seconds as reflected by Table 4-2.

Table 4-2
Time1 and Time2 Fields

Bit #	15-12	11-8	7-4	3-0
TIME0 Field	Not Defined.	Not Defined.	Status.	Unused.
TIME1 Field	2^{28} Seconds.	2^{24} Seconds.	2^{20} Seconds.	2^{16} Seconds.
TIME2 Field	2^{12} Seconds.	2^{8} Seconds.	2^{4} Seconds.	Seconds.
TIME3 Field	10E-1 Seconds.	10E-2 Seconds.	10E-3 Seconds.	10E-4 Seconds.
TIME4 Field	10E-5 Seconds.	10E-6 Seconds.	10E-7 Seconds.	Not Defined.

4.1.15 PACKET "Q" SET DISCIPLINING GAIN

This packet allows the gain and sense of the disciplining process to be set via the host bus. Originally this feature was used for Symmetricom developmental purposes, but it would also be indispensable to anyone attempting to discipline an external oscillator using the TFP. The format is as follows.

byte	1	SOH	
byte	2	"Q"	
byte	3	"0" - "F"	least significant nibble
byte	4	"0" - "F"	most significant nibble
byte	5	sense: "1" = positive, "0" = negative	
byte	6	ETB	

4.1.16 PACKET "S" SET YEAR

This packet allows users to set the year in Modes 0, 1, and 2. This is necessary to get the leap year calculator to function in these modes. After writing the year you must wait at least one full second before reading it back using the "O" packet.

byte	1	SOH
byte	2	"S"
byte	3	years tens
byte	4	years units
byte	5	ETB

This Page Intentionally Left Blank.

CHAPTER FIVE

PROGRAMMING EXAMPLES

5.0 GENERAL

The example code fragments in this chapter are written in the C programming language. The examples have been tested at Symmetricom, and should be transportable to most programming environments. A system dependent base address is defined below where "YYYY" indicates a 64 kbyte page of memory used for A16 data and "SSSS" indicates the SW1 and SW2 switch settings.

```
#define BASE          0xYYYYSSSS
```

The following definitions pertain to FIFO data transfer.

```
#define SOH           0x01
#define ETB           0x17
#define FIFO          (short*)(BASE+0x27)
```

The following global variables are also declared and used throughout this chapter.

```
short   dummy, *readptr, time[5] ;
long    i ;
```

5.1 READING TIME ON DEMAND

The following example reads the time from the TFP registers TIME0 through TIME4 and loads this data into the array time[ ]. The time is latched by reading the TIMEREQ register, and the register is assigned to a global variable. In most cases assignment to a global avoids the possibility that the dummy read operation will be removed by an optimizing compiler (beware).

```
readptr = (short*)(BASE + 0x0A) ;                  /* initialize pointer */
dummy = *readptr++ ;                               /* latch time increment pointer */
for(i=0 ; i<5 ; i++)  time[i] = *readptr++ ;       /* read the time registers */
```

5.2 EXTERNAL EVENT TIME CAPTURE

This example sets up the TFP event capture to occur on a rising edge and generate an interrupt. The time capture lockout mechanism is also used.

```
#define EVENT0              (short*)(BASE+0x16)
#define CMD                 (short*)(BASE+0x24)
#define VECTOR              (short*)(BASE+0x2C)
#define MASK (short*)       (BASE+0x28)
 #define INTSTAT            (short*)(BASE+0x2A)
#define LEVEL               (short*)(BASE+0X2E)
#define UNLOCK              (short*)(BASE+0x20

/* INITIALIZE TFP EVENT HARDWARE */

*CMD = 0x09 ;               /* enable event and lockout */
*VECTOR = 0x40 ;            /* interrupt vector */
*LEVEL = 0x03 ;             /* interrupt level set */
*INSTAT = 0x01 ;            /* clear INSTAT bit */
*MASK = 0x01 ;              /* enable the interrupt */

/* INTERRUPT SERVICE ROUTINE FRAGMENT */

readptr = EVENT0 ;
for(i=0 ; i<5 ; i++)  time[i] = *readptr++;
dummy = *UNLOCK ;           /* release capture lockout */
*INTSTAT = 0x01 ;           /* clear INSTAT bit */
```

5.3 PROGRAM PERIODIC FREQUENCY OF 1,000 HZ

This example uses a generalized send_packet( ) function to program a 1,000 Hz output periodic synchronized to the TFP 1pps epoch.

```
#define ACK             (short*)(BASE+0x22)

void send_packet(char *charptr)
{
*FIFO = SOH ;
while(*charptr) *FIFO = *charptr++ ;       /* load body of packet */
*FIFO = ETB ;
*ACK = 0x81 ;                              /* command TFP & clear ACK */
while(!(*ACK & 0x01)) ;                    /* wait for TFP acknowledge */
}
/* CODE FRAGMENT WHICH SETS PERIODIC */

        send_packet("F500630063") ;                /* 0x0063 = 99 = (100-1) */
```

5.4 SET MODE 1 AND THE MAJOR TIME

This example selects the free running mode and sets the TFP major time, using the “B” packet.

```
send_packet("A1") ;                /* select mode 1 */
*INSTAT = 0x08 ;                   /* clear INSTAT 1pps bit */
while(!(*INSTAT & 0x08) ;          /* wait for 1pps */
send_packet("B123112233") ;        /* set the days through seconds */
```

5.5 SELECT MODE 0 (IRIGB) AND ADVANCE TFP 2.5 MILLISECONDS

The following code fragment selects the mode, timecode, and offset. The last “P" packet is used to disable jamsynchs since the required offset is larger than 990 microseconds. See the “G” packet description for additional details on the jamsynch function.

```
send_packet("A0") ;                /* select mode 0 */
send_packet("HB") ;                /* select IRIGB timecode */
send_packet("G+0025000")   ;       /* advance 2.5 milliseconds */
send_packet("P04") ;               /* disable jamsynchs */
```

This Page Intentionally Left Blank.

CHAPTER SIX

INPUTS AND OUTPUTS

6.0 INPUTS AND OUTPUTS

The front panel I/O for the bc635VME and the bc350VXI (B-size) consists of an LED time and status display, a BNC timecode input, a BNC timecode output, a 15 pin "D" plug, and a 15 pin "D" socket.

The current TFP time *hr:min:sec* is displayed using seven segment LED digits. If the TFP is flywheeling, the digit decimal points are also illuminated. The time display is incremented at 990 milliseconds into the current frame. (One customer measured the LED radix point with a photo diode and reported that it was indeed early!)

Timecode is input using BNC connector J3 or J1-7. Input amplitudes from 0.5 to 5 volts peak to peak are accommodated. Timecode is output on BNC connector J2 or J1-5. The output amplitude is adjustable using ten turn potentiometer VR1 located just below J2 and accessible with the TFP in place. The signals on socket J1 and plug J4 are summarized in Table 6-1 on the following page.

Table 6-1
Socket J1 and Plug 4 Signals

Signals On J1 15 Pin "DS"		Signals On J4 15 Pin "DP"	
Pin	**Signal**	**Pin**	**Signal**
1	*External 10MHz Input or Ovenized Oscillator Output	1	RS-422 Rx(+)
2	Ground	2	RS-422 Rx(-)
3	Strobe Output	3	RS-422 Tx(+)
4	1 PPS Output	4	RS-422 Tx(-)
5	Time Code Output (AM)	5	Ground
6	External Event Input	6	Not Used
7	Time Code Input	7	GPS 1PPS
8	Time Code Return	8	GPS RS-422 1PPS+
9	Oscillator Control Output	9	GPS RS-422 1PPS-
10	Not Used	10	Ground
11	Time Code Output (DCLS)	11	GPS RS-422 Tx(-)
12	Ground	12	GPS RS-422 Tx(+)
13	1,5,10 MHz Output	13	Not Used
14	External 1PPS Input	14	Ground
15	Periodics Output	15	GPS +12 VDC

* Pin 1 is an output when the optional ovenized oscillator is installed.

Table 6-2
TFP Signals on the P2 Connector

TFP Signals On VMEbus P2	
Pin	**Signal**
C1	Time Code Input
C2	Time Code Return
C3	Time Code Output (DCLS)
C4	Time Code Output (AM)
C6	External Event Input
C8	Strobe Output
C9	Periodic Output
C10	External 1PPS Input
C11	1PPS Output
C12	1,5,10MHz Output (Note 2)
C22	10MHz Input
C24	Oscillator Control Output
C18 C20	RS-422 Tx(+) Rx(+)
A18 A20	RS-422 Tx(-) Rx(-)
A26	RS-422 Rx(-) GPS (Note 1)
C26	RS-422 Rx(+) GPS (Note 1)
A28	GPS 1PPS (Note 1)

Note: Hardware Rev. E and later.

Note 2: Hardware Rev. G and later See JP6.

This Page Intentionally Left Blank.

CHAPTER SEVEN
ADJUSTMENTS

7.0 GENERAL

There are only two adjustments on the TFP module, VR1 and VR2. (See figure 1-1 for the location of these potentiometers.)

7.1 TIME CODE PHASE LOCK LOOP ADJUSTMENT

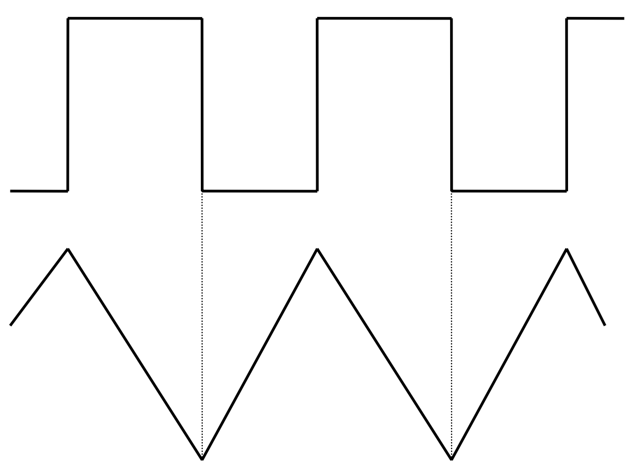
VR2 adjusts the center frequency of the VCO, which locks to the carrier of a modulated input time code. This adjustment is made at the factory and rarely needs adjustment by the customer. This adjustment can be verified and adjusted correctly using a dual trace oscilloscope and a time code input.

- Set the TFP to Mode 0 (Packet "A") and select the appropriate time code format and modulation type (Packet "H").

- Connect channel #1 of the oscilloscope to pin #16 of U19 (XR2212). Connect channel #2 of the oscilloscope to the modulated input time code. Trigger the oscilloscope on the channel #1 input.

- Adjust VR2 so that the positive transition of the TTL signal input to channel #1 is centered on the positive crest of the input sine wave. The negative TTL transition should be centered on the most negative part of the input sine wave. See Figure 7-1 below.

Figure 7-1
Phase Lock Loop Adjustment



7.2 TIME CODE OUTPUT AMPLITUDE ADJUSTMENT

VR1 adjusts the amplitude of the modulated IRIG B output time code. A value of one volt RMS is common as is three volts peak-to-peak on the high cycles. Adjust this value to suit the equipment being driven. The range is zero to twenty-four volts peak-to-peak.

SYMMETRICOM TIMING TEST & MEASUREMENT
3750 Westwind Blvd.
Santa Rosa, California
95403 USA
tel : 707-528-1230
fax : 707-527-6640
info@symmetricom.com
www.symmetricom.com